Take The Mystery Out Of AC Termination

Understanding How to Implement AC Termination, Helps Maintain The Power And Cost Levels In High-Speed Buses.

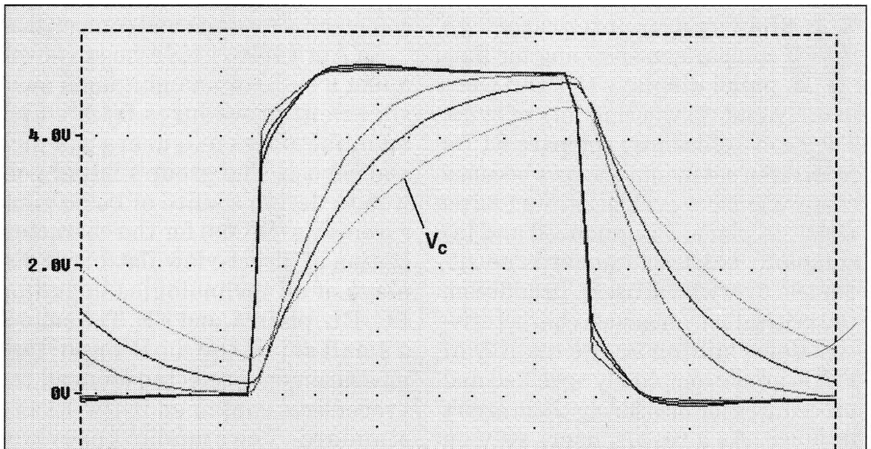
DR. JOHN NEMEC, California Micro Devices Corp., 215 Topaz St., Milpitas, CA 95035; (800) 325-4966 or (408) 263-3214; Internet: http://www.calmicro.com.

Today's high-speed bus applications require the use of terminations to enable proper system operation. System designers can select from various termination options to achieve the optimal balance between performance and cost. Various choices include standard parallel termination, series-resistor termination, dual or Thévenin termination, diode termination, and ac termination. Of these choices, ac termination has the potential to maintain signal integrity while reducing power consumption in high-speed applications.

High-speed buses using a point–to–point configuration of drivers and sources are tailor-made for the ac-termination alternative. Results of the analysis show that the capacitor can charge almost completely, and still provide effective termination. In addition, the relatively small current requirement of ac termination results in significant power supply cost savings.

In multidrop environments (both in a single driver with multiple receivers, and multiple drivers with multiple receivers), ac termination has some limitations. Depending on the signal levels required, ac termination may not be able to achieve the desired signal levels at any arbitrary point along the line, unless the line is short. Other termination types may be better suited for these designs, and careful analysis is required.

In high-speed systems, the signal-edge rates and bus speeds approach the propagation delay of the bus, making appropriate selection and termination a necessity. Many high-speed systems also use CMOS devices, or similar logic, which have large swings in driver output signal levels. Combined with low-impedance buses (typically 47 Ω to 70 Ω), common in practical pc-board traces, using parallel or Thévenin termination for a transmission line in these environments has significant disadvantages. Specifically, the added power needed due to a constant dc current flow through the ter-



1. Based on the requirement to make the overshoot reach the driver's open circuit voltage, the signal amplitude maintains acceptable noise margins, using values of R_S = 10, 15, and 20 W (a). In addition, the overshoot and edge–to–edge interaction is held to a minimum (b).

mination resistor can be a serious drawback. In larger systems, several watts of power may be wasted, or additional cost may be incurred to provide a separate power supply.

The ac termination alternative consists of a resistor in series with a capacitor. The resistor performs the termination and the capacitor blocks the dc average current, saving considerable power. Additionally, ac termination can match the bus impedance, like pure resistor terminations, but with minimal signal reflection. And, it can be placed at the end of the transmission line while maintaining the signal integrity, like parallel and Thévenin terminations.

Optimum Design

Optimum ac termination for a point–to–point application is achieved when the peak amplitude of the first signal reflection on the transmission line equals the driver's open-circuit voltage. Meeting this criterion results in a terminated signal with sufficient amplitude to achieve acceptable noise margins, while keeping signal overshoot and edge–to–edge interaction to a minimum. The design involves the calculation of the capacitance value for the ac termination.

When driver rise times are relatively small and the bus propagation delay is significantly less than the signal edge–to–edge times, equation (1) can be applied *(see sidebar p. XX)*, where t_D = propagation delay (ns); Z_0 = characteristic impedance of the transmission line; R_S = source impedance; and G = source reflection coefficient.

Solving for the optimal termination capacitance value gives rise to equation (2) in the sidebar.

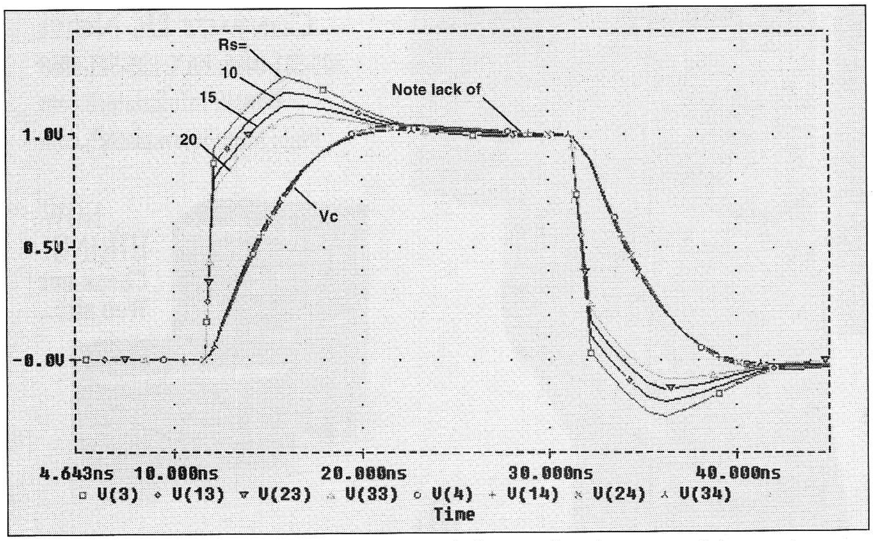
In a practical example, a system employs a 66-MHz data bus which must be terminated. The bus impedance, including loading effects for this system, is 60 Ω. The bus has a one-way 0.8-ns propagation delay. The driver on the bus has an internal 10-Ω impedance, and rise and fall times equal to 600 ps. Signal edge–to–edge time is 15 ns.

Inserting the values from the above example and multiplying the propagation delay by 1000 to obtain a result in picoFarads gives a termination capacitance value shown in equation (3) in the sidebar.

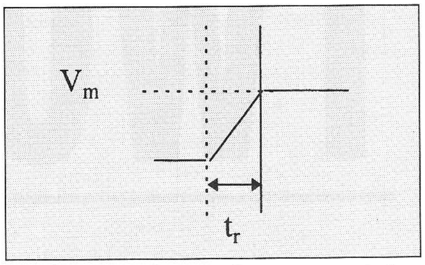
Simulation Results

When this termination capacitance is plugged into a Spice simulation, the signal amplitude maintains acceptable noise margins, while keeping overshoot and edge–to–edge interaction to a minimum *(Fig. 1a and b)*.

Note that the terminated waveform rises to some initial voltage, which is determined by the driver voltage and the ratio of the driver's internal impedance to the bus impedance. The capacitor begins to charge, causing a reflection, and the termination voltage begins to rise. The waveform then reaches a peak, after which it remains relatively flat. This plateau indicates that reflections are minimized. Using larger or smaller capacitor values results in ringing or edge–to–edge interactions.



2. The square of the voltage across the resistor, which is equal to the square of the area between the capacitor and termination voltage, divided by the resistance is equal to the power dissipated in an ac termination resistor. In this simulation, $Vcb(2t_D)/V_S=1$.



3. When a signal is sent down a transmission line with ac termination, it can be modeled as a linear ramp going from 0 to V_m with a rise time of t_R. At the end of t_R, the signal remains at V_m.

There may be a timing budget impact depending on the desired noise margins. The signal waveform rises or falls to some initial value and then continues as the capacitor charges or discharges. If this initial amplitude is within acceptable noise margins, then ac termination has no more impact on the timing budget than a standard parallel termination. If, however, the initial amplitude isn't sufficient, the timing budget must include the additional time required for the signal to reach the required level.

If the capacitor is made excessively large, it can retain a significant charge from edge–to–edge, causing a walking baseline that's duty-cycle dependent. Thus, for short duty cycles (for either the logic high or low portion of the signal), edge–to–edge interaction is a concern. Effects on the waveform would appear as a significant change in the initial voltage reached just after the edge arrival, and as a longer time to reach the required signal levels.

A Low-Power Solution

The power dissipated in an ac termination resistor equals the square of the voltage across the resistor divided by the resistance. This figure is equal to the square of the area between the capacitor and termination voltage *(Fig. 2)*. Note that power is dissipated only when transitions occur, and therefore, power is duty-cycle dependent. Also, the area between the capacitor and termination voltage is about 25% to 30% of the whole area of the termination voltage. Because power dissipation is based on the square of the voltage, ac termination will consume less than 10% of the power consumed by parallel termination under the same conditions.

Based on this analysis, the system designer can charge the capacitor almost completely while providing effective termination. The signal current through the termination resistor can be a small fraction of the current through a parallel termination. (Parallel termination also may include dc power-supply current.) This design can significantly reduce the power-supply cost.

Point-to-Point Applications

For practical ac-termination applications, the termination resistor value equals the transmission-line impedance. The interplay between the capacitance and other system conditions makes the termination-capacitance value more difficult to determine. Whether a design can benefit from ac termination requires determination of specific performance issues and factors which may contribute to the loss of signal integrity. This analysis considers the effects of signal rise time, reflections, overshoots, and undershoots in determining an optimal ac termination design.

Rise-Time Effects

The system designer must know under which conditions a signal edge retains its integrity and timing position. A slow edge may invalidate the capacitance value computed in the optimum design. A signal launched down a transmission line with ac termination can be modeled as a linear ramp from 0 to some maximum voltage, V_m, with a rise time of t_R, after which the signal remains at V_m *(Fig. 3)*. V_m may be smaller than the driver amplitude due to the driver's source impedance. Assume that the driver is relatively stiff with a source impedance, RS, less than the characteristic impedance of the transmission line, Z_0. The launched signal amplitude, V_m, is related to the open-circuit driver signal amplitude, V_S, by equation (4) in the sidebar, where Z_0 = the transmission line's characteristic impedance; R_S = the source impedance; and G = the source reflection coefficient.

In the region where the linear ramp is occurring *(Fig. 4)*, the reflected voltage, V_r, is shown in equation (5) in the sidebar, where t_R = rise time; C = termination capacitance; and V_0 = any initial voltage on the capacitor due to previous conditions.

The reflected voltage in Region 1 starts at 0 (when $V_0 = 0$) and increases. The total voltage at the termination will be larger than the incident voltage. The effect of ac termination is to steepen the edge rate slightly and reduce the apparent arrival time of the signal.

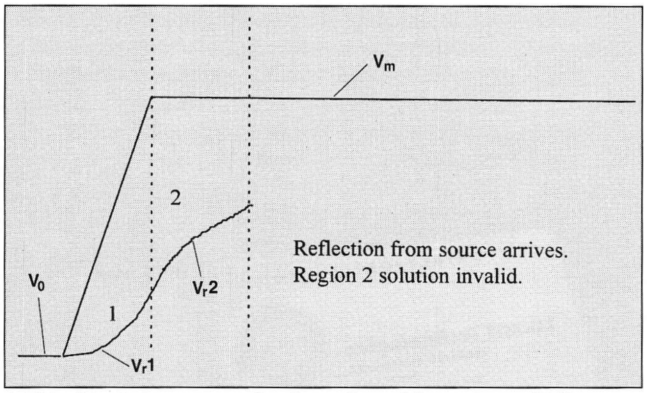
In Region 2, the initial ramp is completed and the reflected voltage is shown by equation (6) in the sidebar. In this equation, the time origin is at the beginning of Region 2 and is not the same as t in the previous equation. For very small rise times, t_R can be taken to 0, Regions 1 and 2 combine, and the reflected voltage is shown in equation (7) in the sidebar, where V_{ra} is the reflected voltage using a zero rise-time approximation. The zero rise-time approximation is valid if $Vr1(t_R)$ is small compared to V_m.

Using the series expansion for the exponential function, $Vr1(t_R)/V_m$ is on the order of $t_R/4Z_0C$. This suggests that under most circumstances (where $t_R < Z_0C/2$), the rise time of the driver signals is fast enough to have negligible affect on termination performance. Using this result, the driver rise time is neglected and the equation for the optimum value of capacitance can be derived.

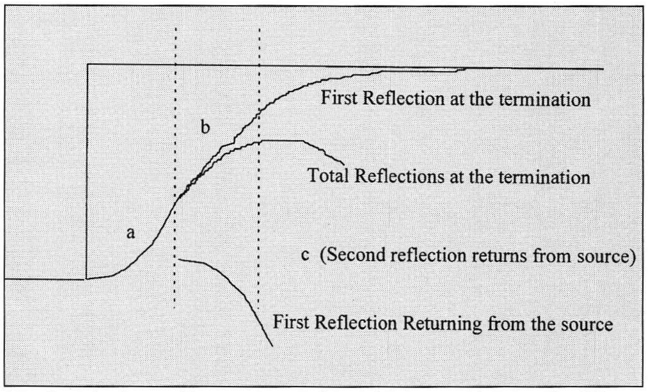
The result from the previous equation indicates that the reflected voltage is rising toward V_m, with a time constant of $2Z_0C$. The total voltage at the termination end is rising toward $2V_m$. The reflected signal will travel back to the source, be reflected, and return to the termination end *(Fig. 5)*.

The reflection from the source will arrive at the termination end of the line, change the voltage waveform, and cause another reflection back to the source. Because the reflection coefficient at the source is negative (low source impedance), the reflection from the source will be opposite in polarity from the reflection at the termination. The series of reflections should quickly reduce in amplitude and die away in a manner comparable to what happens in a close, but not exact, ac termination condition. The largest amplitude overshoot will occur with the first reflection at the termination end, and (approximately) when this reflection arrives back from the source. The peak amplitude above V_m is shown in equation (8) in the sidebar.

A Spice simulation of Vr_{max} for various values of Z_0C gives a comparison of the peak overshoot from the simulation versus the predicted values from the previous equation *(Fig. 6)*. Note



4. This plot shows an example of signals with finite rise and fall times at the end of an ac-terminated transmission line.



5. When the first reflection returns from the source, the signal will be reflected and return to the termination end.

that the result is in terms of the launched signal amplitude, V_m (not the open-circuit driver amplitude), and that the overshoot is measured with respect to V_m.

It's desirable to keep the overshoot low to prevent the forward biasing of semiconductor structures in components connected to the line. Moreover, having large overshoots indicates large reflections which could upset the signal integrity, creating an error in a clocked-in value. Additionally, large reflections will be present at a subsequent signal transition, disrupting the signal integrity associated with the signal's new state.

Solving for Z_0C gives the minimum capacitance value required to limit the overshoot to Vr_{max} as shown in equation (9) in the sidebar.

Determine The Optimum Value

System designers also must consider the effect of reflections and the capacitor's charge state on subsequent signal transitions. When a new transition occurs, the capacitor will be charged to some level determined by the dynamics of the previous transition. Also, reflections from the previous transition may not have summed to an insignificantly small value. For example, in a circuit with a very large capacitor, the capacitor voltage changes very little from transition to transition. The capacitor will eventually charge to the signal's average level. Reflections will be negligible, and the voltage at the termination point will be ideal. However, the source generally isn't stiff and may have an internal impedance on the order of 10 Ω or more. For a 50-Ω line, the signal amplitude will be 5/6 of the open-circuit drive level or a little over 4 V p-p for a 5-V driver. A large termination capacitor will tend to charge to about 2.5 V (for a 50% duty cycle), and the signal swing at the line's termination end will be about 0.5 V to 4.5 V. The results are a reduced signal amplitude and a decrease in the logic 0 noise margin. These drops suggest a very large capacitor isn't suitable for practical source impedances. In addition, this situation makes these signals duty-cycle dependent. As the duty cycle changes, the average charge on the capacitor changes, resulting in a wandering baseline that reduces the noise margin to the input logic thresholds.

TABLE 1

R_S/Z_0	t_D/Z_0C
0.1	0.105
0.2	0.223
0.3	0.357
0.4	0.511
0.6	0.916

TABLE 2

R_S/Z_0	Z0C/tD min.
0.1	2.05
0.2	1.80
0.3	1.55
0.4	1.35

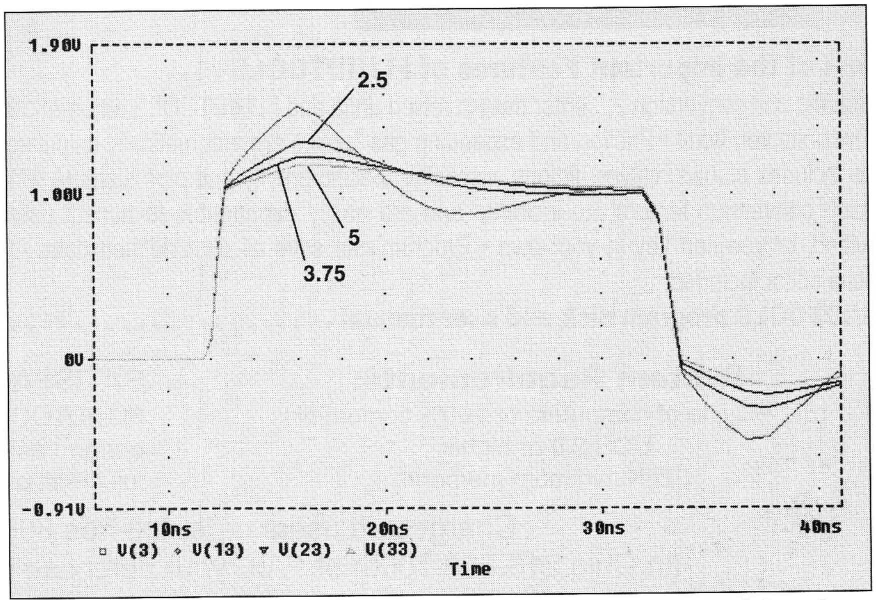
An overshoot may be desirable in some specific situations. Designers could use the overshoot to make up for amplitude loss due to the source impedance. Complete analysis of the entire transient may be required. Moreover, only specific regions in the signal waveform may be of interest. For example, the overshoot could ensure that the noise margin of a data line is within a set-up and hold time around a clock edge, and the signal may be allowed to violate the noise margin elsewhere. Note that the peak overshoot occurs at $2t_D$ after the signal's rising edge, impacting the timing budget and possibly limiting the applicability of this technique. One must wait until the overshoot brings the signal to the appropriate level, which could be as long as $2t_D$. Determining the maximum value of capacitance in all these cases requires simulation.

Edge-To-Edge Interaction

Meeting the criterion that the first overshoot peak reach the driver's open-circuit voltage (V_S) drives the termination to the steady-state voltage. If the driver were to maintain its state indefinitely, the capacitor would charge to V_S and all reflections would die away; there would be no current in the transmission line and the termination voltage would be at V_S. Designing such that the termination voltage reaches V_S is an optimum condition for reaching a quiescent state and for minimizing edge–to–edge interaction. This solution is a best-case scenario, giving the fastest rise time-signal with no overshoot. The analysis and simulation results confirm that setting the capacitance value such that the peak overshoot is equal to the open circuit driver provides an optimum solution for reducing noise margins and minimizing edge–to–edge interactions. By imposing this requirement, the minimum value of t_D/Z_0C can be calculated using the optimum design equation *(Table 1)*.

Multidrop Environments

When multiple receivers are distributed along the line, it is desirable



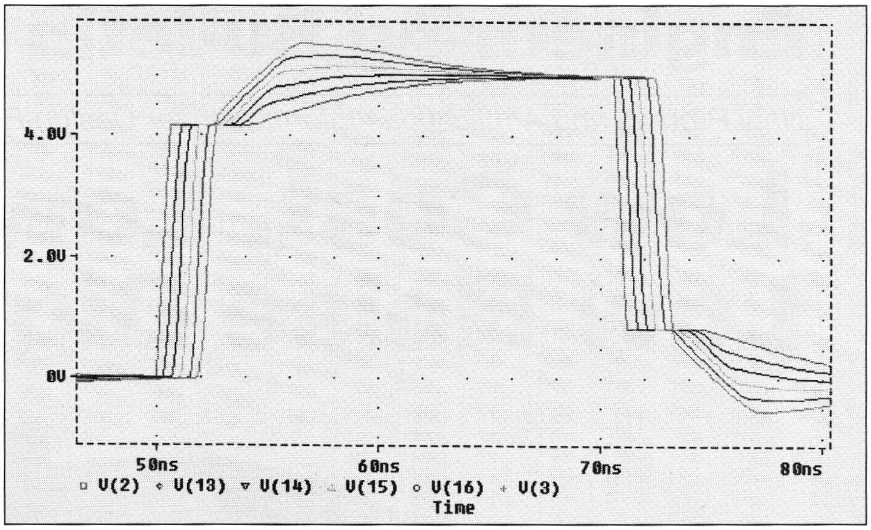
6. When VR_{max} is solved for various values of Z_0C, the result gives a comparison of the peak overshoot from the simulation versus the predicted values. In the plot, $V_0 = 0$ and $R_S = 0$.

to have signal integrity at each receiving point. With optimum termination and a 10-Ω source resistance, R_S, the curves show the signal at equally spaced points along the transmission line *(Fig. 7)*.

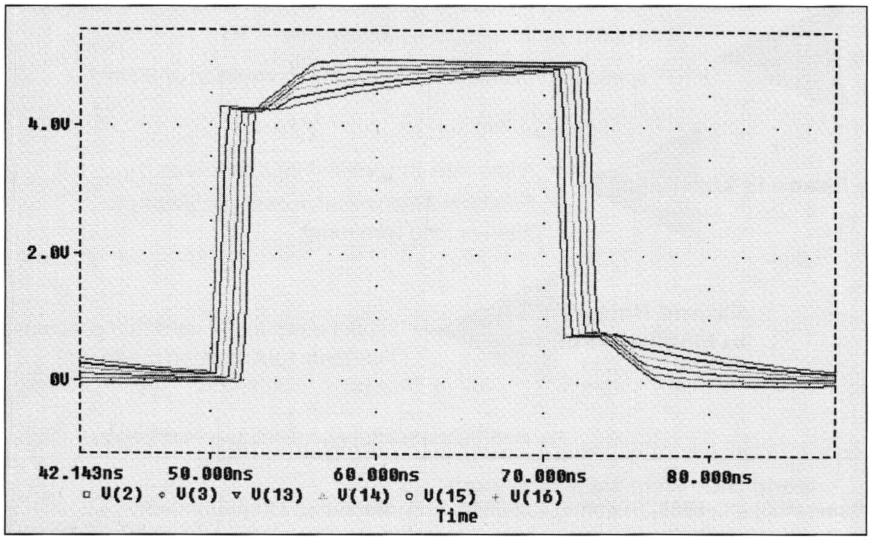
The left-most curve at the rising edge is the signal at the driver, and the curves at successively later times are at positions along the transmission line from the source to the termination. Note, in particular, the first curve (driver end)—the signal rises rapidly to V_m and then rises to V_S only after many t_D times. Successive signals down the transmission line show incremental improvement reaching the optimum termination at the furthest point on the line. The results indicate that, while the signal overshoots are virtually nonexistent, the time it takes for a signal to reach a given level above V_m increases as a receiver moves toward the driver end of the line.

These simulations present three interesting results: as expected, the signal level is initially better with lower source impedance; after about $4t_D$, the signals under larger source impedance reach higher levels faster than signals under smaller source impedance; and all signals appear to monotonically increase to the driver's open circuit voltage. If a time constant is attributed to the rising curves, it is roughly Z_0C by empirical determination.

With multidrop receivers, depending on the signal level needed at a particular time after the signal transition, ac termination may have limited effectiveness. The signal's ability to achieve required amplitudes at a receive point at or near the line's driver end is limited by several line delays, t_D, and the Z_0C product. Even with these limitations, ac termination may be suitable for short buses and loads clustered toward the end of the line opposite the driver.



8. Reducing the termination capacitance is one way to raise the signal levels (while accepting an overshoot at the termination end) and improve the rate at which the signal at the other points on the line rises to the required level.



7. This simulation shows signals at multiple receive points along a line when employing the optimum termination and a 10-W source resistance

An approach to raising the signal levels, if required, is to reduce the termination capacitor value, accept an overshoot at the termination end, and improve the rate at which the signal at the other points on the line rise to the required level *(Fig. 8)*. The receivers in about the last half of the bus see signal levels at or above the driver's open-circuit voltage within $3t_D$. This improvement is considerable over the optimum termination at the expense of overshoot at points near the termination end of the line.

System designers must make a trade-off in tolerating overshoot above the optimum design level (and some ringing) to ensure improved signal level toward the driver end. This technique also could impact the timing budget. Note that the time it takes a signal (at some given point along the line) to rise (or fall) to a given level could exceed the time it takes for the terminated signal to reach its peak. As a result, the clock edge would be required to be moved later in time to guarantee successful clocking-in of the signal. The situation improves as the driver source impedance decreases. This decrease allows the signal amplitude to reach the desired level without compromise, providing that a low enough impedance can be achieved in the driver. Since multiple reflections are involved, simulation is the best approach in selecting the optimum ac-termination capacitor value.

Even though the smaller source resistances improve the levels, the signal's apparent rise time at the line's driver end actually gets slower. If the source resistance must be so greatly increased as to require a series termination at the driver, and no termination at the opposite end of the transmission line, it's better to select another termination alternative.

When the termination is at the opposite end of the line from the driver, ac termination can be used in a single source, multidrop situation. Because the desired signal characteristics degrade as the receivers move from the termination end to the driver end, it's advantageous to have the receivers clustered near the termination end of the line. To achieve good signal characteristics at the receiver closest to the driver, the termination capacitance must be lowered to achieve acceptable signal levels within a given time from the signal edge. This design comes at the expense of overshoot at the termination end. Moreover, the section of the line with the clustered receivers will have a lower characteristic impedance than the unloaded section of the line between the driver and the first receiver. This technique requires that the line be designed for different unloaded impedance in these two line sections so that when loaded, the line impedance will be constant over the entire length.

Multiple Drivers On The Line

When multiple drivers or sources exist along the transmission line, it's appropriate to terminate both ends of the line. As indicated in the multidrop analysis, the optimum termination capacitance is determined by the line's propagation delay. However, as the source moves along the line, the optimum capacitance value changes, and the termination dynamics change as a result of the driver's position. No optimum solution exists for multiple driver configurations, only trade-offs, unless the line is short. Simulation is the simplest way to determine system performance *(Fig. 9)*.

In the multidrop and multisource environments, it was observed that the signal amplitude near the driver took a longer time to rise to its final level than the signal at the termination end. If the initial amplitude of the signal is sufficient for the required noise margin, then the optimum design can be used. However, if this amplitude is not sufficient, the timing budget must be adjusted accordingly.

To minimize the adjustment, it may be desirable to let the signal at the termination end overshoot the

EQUATIONS

$$\frac{t_D}{Z_0C} = \ln\left(\frac{1-G}{-2G}\right) = \ln\left(\frac{Z_0}{Z_0-R_S}\right) \quad (1)$$

$$C = \frac{t_D}{Z_0 \times \ln\left(\frac{Z_0}{Z_0-R_S}\right)} \quad (2)$$

$$C = \frac{0.8\text{ns} \times 1000}{60\Omega \times \ln\left(\frac{60\Omega}{60\Omega - 10\Omega}\right)} = 73\text{pF} \quad (3)$$

$$V_m = V_s\frac{Z_0}{R_S+Z_0} = V_s\frac{1-G}{2} \quad (4)$$

$$Vr1(t) = -2Z_0C\frac{V_m}{t_r} + V\frac{t}{t_r} + \left(\frac{V_0}{2} + 2Z_{0C}\frac{V_m}{t_r}\right)e^{\frac{-t}{2Z_0C}} \quad (5)$$

$$Vr2(t) = V_m + \left(\frac{1}{2}Vr1(t_r) - V_m\right)e^{\frac{-t}{2Z_0C}} \quad (6)$$

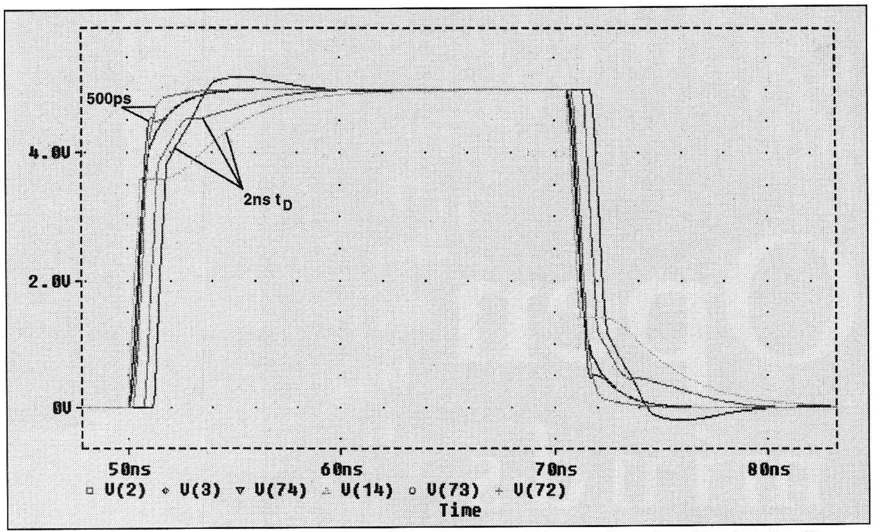
$$Vra(t) = V_m + \left(\frac{1}{2}V_0 - V_m\right)e^{\frac{-t}{2Z_0C}} \quad (7)$$

$$Vr_{max}(t) = V_m + \left(\frac{1}{2}V_0 - V_m\right)e^{\frac{-2t_D}{2Z_0C}} \quad (8)$$

$$Z_0C = \frac{t_D}{\ln\left(\frac{V_m}{V_mVr_{max}}\right)} \quad (9)$$

$$Vb(t) = (1+2G)V_m - 2GV_m\frac{t}{2Z_{0C}}e^{\frac{-t}{2Z_0C}} - 2V_m\left(G + e^{\frac{-t}{2Z_0C}}\right) \quad (10)$$

$$Vcb(2t_D) = 2V_S\left[1 - e^{\frac{-4t_D}{2Z_0C}} + G\left(1 - e^{\frac{-2t_D}{2Z_0C}}\right) - G\frac{2t_D}{2Z_{0C}}e^{\frac{-2t_D}{2Z_0C}}\right]\left(\frac{1-G}{2}\right) \quad (11)$$



9. In a multidriver environment with short lines, ac termination can be quite effective. In this example, the driver resistance is 10 W and the termination capacitors at each end of the line are adjusted to give the best results.

driver's open-circuit voltage so as to gain signal amplitude elsewhere.

Knowing that reducing the capacitor value increases the reflections, it's possible that subsequent reflections may cause the signal at the termination to fall below its final value. The analysis in this section seeks a capacitor value that is smaller than that given by the initial calculation for C, thereby increasing the signal amplitude at the multidrop points, and preventing undershoot (signal going lower than the final value due to reflections).

When the reflection returns from the source and arrives at the line's termination end, the charging conditions on the capacitor change. To simplify this analysis, the initial capacitor voltage, V_0, is taken to be zero. The reflection returns from the source delayed by $2t_D$ and multiplied by the source reflection coefficient, G. The equation for the voltage at the termination (less the incident voltage, V_m) in the region after the reflection from the source arrives at the termination end ($t>2t_d$) is shown in equation (10) in the sidebar.

In this equation, t is referenced to the beginning of this region. The results show that the overshoot voltage will decline toward the value $(1+2G)V_m$. With a large overshoot, the large reflection can return (inverted), and at some time in the future cause the signal to undershoot the desired value. This undershoot may occur at any time following the initial overshoot peak. Though it's difficult to do a complete analysis, it's reasonable to suppose that if the capacitor voltage ever rises above V_S, the termination effect is reduced to the point that large amplitude reflections will continue. This result suggests that prolonged ringing can be suppressed if the capacitor voltage is not permitted to rise above V_S during Region b *(Fig. 4, again)*. Examining the capacitor voltage in Region b, the voltage at the end of the validity of Region b ($t = 2t_D$) is defined by equation (11) in the sidebar.

This voltage is in terms of the open-circuit source voltage, V_S. By requiring that the capacitor voltage never rise above V_S (i.e., keeping the termination voltage from undershooting V_S), another criterion is set for determining the minimum value of the capacitor. If it's desirable to allow larger then optimum overshoots for multidrop situations, using this criterion will minimize undershooting the steady-state level at the termination end *(Table 2)*.

Dr. John Nemec, director of applications at California Micro Devices, holds a Ph.D. in Electrical Engineering from the University of Houston.

HOW VALUABLE	CIRCLE
HIGHLY	532
MODERATELY	533
SLIGHTLY	534

Looking for Consultants?

IEEE-USA's Directory of Electrotechnology Consultants is a must for any company or institution that uses technical or management consultants. The **Directory** lists independent consultants who are operating as sole practitioners or in small businesses and also gives detailed information regarding specific areas of expertise.

Prepared by the Coordinating Committee of the Alliance of IEEE Consultants' Networks, the **Directory** is available as a searchable database on the Web at <http://www.ieee.org/usab/DOCUMENTS/CAREER/AICN/dbform.html>.

Or, for a free hard-copy version, contact Bill Anderson at:

THE INSTITUTE OF ELECTRICAL
AND ELECTRONICS ENGINEERS, INC.

IEEE United States Activities
1828 L Street, NW, Suite 1202
Washington, DC 20036-5104

Phone: 202-785-0017 Fax: 202-785-0835
Email: w.anderson@ieee.org